FACULTY OF ENGINEERING & TECHNOLOGY

Effective from Academic Batch: 2022-23

Programme: **BACHELOR OF TECHNOLOGY (Electronics and Communication)**

Semester: **VI**

Course Code: **202060603**

Course Title: **VLSI Design**

Course Group: **Professional Core Course**

Course Objectives: This course will provide an opportunity to the students to learn about VLSI design and analysis with reference to MOSFET. To learn basic MOS Circuits, CMOS Circuits and CMOS process technology. To learn techniques of chip design using programmable devices.

Teaching & Examination Scheme:

Contact hours per week			Course Credits	Examination Marks (Maximum / Passing)				
				Theory		J/V/P*		
Lecture	Tutorial	Practical		Internal	External	Internal	External	Total
3	0	2	4	50/18	50/17	25/9	25/9	150/53

* **J**: Jury; **V**: Viva; **P**: Practical

Detailed Syllabus:

Sr.	Contents	Hours
1	**Introduction and Fabrication of MOSFET:** VLSI Design Flow, Design hierarchy, Design Methodology, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.	06
2	**Metal Oxide Semiconductor Transistor:** Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure & Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling & small-geometry effects, MOSFET capacitances	10
3	**Static characteristic and switching characteristic of MOS Inverters:** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement & Depletion type MOSFET load), CMOS Inverter, Delay-time definitions, Calculation of Delay times, Inverter design with delay constraints, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters	10

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4	**MOS Combinational, Sequential and Dynamic logic circuits:** Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, Design of logic blocks – Adder, Multiplier and Shifter. CMOS Transmission Gates (TGs). Behavior of Bistable elements, The SR latch circuit, Clocked latch & Flip-flop circuit, CMOS D-latch & Edge-triggered flipflop, Principles of pass transistor circuits, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, Domino Logic.	**12**
5	**Design for testability and FinFET:** Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques, built-in Self-Test (BIST) techniques, current monitoring IDDQ test. Limitation of CMOS technology, SOI (Silicon on Insulator), FinFET: structure, output characteristics	**07**
		45

List of Practicals / Tutorials:

1	Introduction to programmable devices (FPGA, CPLD), Hardware Description Language (VHDL/Verilog), and the use programming tool.
2	Implementation of basic logic gates and its testing.
3	Implementation of adder circuits and its testing.
4	Implementation 4 to 1 multiplexer and its testing.
5	Implementation of 3 to 8 decoder and its testing.
6	Implementation of 8 to 3 priority encoder and its testing.
7	Implementation of J-K and D Flip Flops and its testing.
8	Simulation of CMOS Inverter using SPICE for transfer characteristic.
9	Simulation and verification of two input CMOS NOR gate using SPICE.
10	Implementation and simulation of given logic function using dynamic logic.
11	Introduction to Altera DE1/Xilix Spartan board.

Reference Books:

1	Sung-Mo-Kang, Usuf Leblebici, **CMOS Digital Integrated Circuits, Analysis and Design**, Revised 4th edition, Tata McGraw Hill, 2018.
2	D. A. Pucknell, K. Eshraghian, **Basic VLSI Design**, 3rd Edition, PHI.
3	Mead C and Conway, **Introduction to VLSI Systems**, Addison Wesley
4	Jan M. Rabaey, Anantha Chandrakasan, Borivoje. Nikolic, **Digital Integrated Circuits: A Design Perspective**, 2nd Edition, Pearson, 2016.
5	Brown and Vranesic, **Fundamentals of Digital Logic Design with VHDL,** Tata McGraw Hill, 2008.
6	Neil H.E. Weste, David Money Harris, **CMOS VLSI Design: A Circuits and Systems Perspective**, 4th Edition, Pearson, 2017
7	Samir Palnitkar, **Verilog HDL: A Guide to Digital Design and Synthesis,** 2nd Edition, Prentice Hall, 2003.

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8	Jean-Pierre Colinge, **FinFETs and Other Multi-Gate Transistors**, , Springer New York, NY, https://doi.org/10.1007/978-0-387-71752-4

Supplementary learning Material:	
1	NPTEL Course on VLSI Design, IIT Bombay Prof. A.N. Chandorkar
2	NPTEL Course on NOC: CMOS Digital VLSI Design, IIT Roorkee Prof. Sudeb Dasgupta

Pedagogy:

- Direct classroom teaching
- Audio Visual presentations/demonstrations
- Assignments/Quiz
- Continuous assessment
- Interactive methods
- Seminar/Poster Presentation
- Industrial/ Field visits
- Course Projects

Internal Evaluation:

The internal evaluation comprised of written exam (40% weightage) along with combination of various components such as Certification courses, Assignments, Mini Project, Simulation, Model making, Case study, Group activity, Seminar, Poster Presentation, Unit test, Quiz, Class Participation, Attendance, Achievements etc. where individual component weightage should not exceed 20%.

Suggested Specification table with Marks (Theory) (Revised Bloom's Taxonomy):

Distribution of Theory Marks in %						**R**: Remembering; **U**: Understanding; **A**: Applying; **N**: Analyzing; **E**: Evaluating; **C**: Creating
R	**U**	**A**	**N**	**E**	**C**	
10	25	10	20	20	15	

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Course Outcomes (CO):

Sr.	Course Outcome Statements	%weightage
CO-1	Understand physics of MOSFET and hence utilize this in analysis of basic building block of digital integrated circuits.	**25**
CO-2	Identify and analyze the recent trends in VLSI Technologies, advance technologies like FinFET and Design methodologies.	**25**
CO-3	Interpret & evaluate dynamic logic concept and hence construct high density and high-performance digital circuits design. Understand advanced MOSFET structures	**25**
CO-4	Design combinational and sequential circuits using various topologies that realizes digital functions of given specification	**25**

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Curriculum Revision:	
Version:	2.0
Drafted on (Month-Year):	June -2022
Last Reviewed on (Month-Year):	-
Next Review on (Month-Year):	June-2025

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